REMARKS

Claims 1-17 are pending in the present application. Reconsideration and allowance of pending claims 1-17 in view of the following remarks are requested.

In the Office Action dated September 27, 2004, the Examiner has *finally rejected* claims 1-17 pending in the application on the basis of new ground(s) of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated September 27, 2004.

A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection dated September 30, 2003 (37 CFR §1.116(c)). The new reference is Rompaey et al. (USPN 5,870,588) (hereinafter "Rompaey"), which is for the first time brought to Applicant's attention by means of the present *final rejection* dated September 27, 2004. The new reference, i.e. Rompaey, was not cited in the present application prior to the instant final rejection. Since Rompaey is a reference upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments, which are necessitated due to the newly cited reference, Rompaey.

A. Rejection of Claims 1, 2, 7, 11, 12, and 15 under 35 USC §103(a)

The Examiner has rejected claims 1, 2, 7, 11, 12, and 15 under 35 USC §103(a) as being unpatentable over "Synthesis and Simulation of Digital Systems Containing

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Interacting Hardware and Software Components," ACM/IEEE, 1992, pp. 225-230, by Gupta et al. ("Gupta") in view of Rompaey. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Gupta and Rompaey, singly or in any combination thereof.

The present invention, as defined by independent claims 1, 7, 11, 12, and 15, recites, among other things, running a unified simulation of a system design and an application program as a single process and allowing the application program to be loaded into a memory component for simulation. As disclosed in the present application, the present invention integrates hardware and software components of a system design in a single unified simulation environment. As disclosed in the present application, use of a system model in a unified simulation allows application software to be loaded into a memory component in the system model. As disclosed in the present application, a low level operating system application may be loaded onto a memory component in the simulation environment, for example. As disclosed in the present application, a processor component of the system model may simulate the operation of the operating system during the simulation by executing the instructions of the operating system. As a result, in the present invention, a single simulation environment can advantageously simulate both the hardware components (memory and processor) as well as a software component (the operating system application). Also, since the unified simulation environment runs

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as one process, simulation time is advantageously reduced and debugging is advantageously simplified.

In contrast to the present invention as defined by independent claims 1, 7, 11, 12, and 15, Gupta does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process and allowing the application program to be loaded into a memory component for simulation. Gupta specifically discloses an event-driven simulator (Poseidon) that performs concurrent simulation of multiple functional models implemented either as a program or as application-specific hardware. See, for example, Gupta, pages 228-229. In Gupta, the software component is compiled into the assembly code of the target microprocessor. See, for example, Gupta, page 229. In Gupta, the hardware component of the system design can be simulated either before or after the structural synthesis phase. See, for example, Gupta, page 229. However, Gupta fails to teach, disclose, or suggest a unified simulation of a system design and an application program that runs as a single process, as specified by independent claims 1, 7, 11, 12, and 15. Also, Gupta fails to teach, disclose, or suggest an application program to be loaded into a memory component of the system design for simulation.

In contrast to the present invention as defined by independent claims 1, 7, 11, 12, and 15, Rompaey does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process and allowing the application program to be loaded into a memory component for simulation. Rompaey specifically

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discloses a simulation of a digital system including software subsystems that are executed on one or more hardware subsystems. See, for example, Rompaey, column 6, lines 36-49. In Rompaey, the hardware subsystems comprise any one or more of processor cores, off-the-shelf components, custom components, ASICs, processors, and boards, while the software subsystems comprise machine instructions for the hardware subsystems. See, for example, Rompaey, column 6, lines 49-53.

Rompaey further discloses removing inter-process communication with remote-procedure-call semantics between a plurality of processes by "merging the plurality of processes." See, for example, Rompaey, column 7, lines 24-27. However, "merging the plurality of processes" referred to in Rompaey is not the same as running a unified simulation of a system design and an application program in a single process, as specified in independent claims 1, 7, 11, 12, and 15. In Rompaey, a "process" is a container for a number of host language encapsulations of a component. See, for example, Rompaey, column 11, lines 40-41. Thus, Rompaey fails to teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process, as specified in independent claims 1, 7, 11, 12, and 15. Also, Rompaey fails to teach, disclose, or suggest allowing an application program to be loaded into a memory component of a system design for simulation. Thus, Rompaey fails to cure the basic deficiencies of Gupta discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is not suggested

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disclosed, or taught by Gupta and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Gupta and Rompaey. Thus claim 2 depending from independent claim 1 is, *a fortiori*, also patentably distinguishable over Gupta and Rompaey for at least the reasons presented above and also for additional limitations contained in the dependent claim.

B. **Rejection of Claims 1-17 under 35 USC §103(a)**

The Examiner has further rejected claims 1-17 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,615,357 to Loran P. Ball ("Ball") in view of Rompaey. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Ball and Rompaey, singly or in any combination thereof.

In contrast to the present invention as defined by independent claims 1, 7, 11, 12, and 15, Ball does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process and allowing the application program to be loaded into a memory component for simulation. Ball is directed to a system and method for verifying processor performance. Ball specifically discloses a simulator that employs a benchmark program, such as benchmark program 50, to generate performance statistics. See, for example, column 9, lines 27-32 and Figure 5A of Ball. However, Ball fails to teach, disclose, or suggest a running a unified simulation of a

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system design and an application program as a single process, as specified in independent claims 1, 7, 11, 12, and 15.

Ball further discloses simulated CPU 30, which may receive instructions from Random Access Memory ("RAM") 32 and trace file 43, in simulator 28. See, for example, column 6, lines 54-58 and Figure 2 of Ball. However, Ball fails to teach, disclose, or suggest allowing an application program to be loaded into a memory component of a system design for simulation, as also specified in independent claims 1, 7, 11, 12, and 15.

As discussed above, in contrast to the present invention as defined by independent claims 1, 7, 11, 12, and 15, Rompaey does not teach, disclose, or suggest running a unified simulation of a system design and an application program as a single process and allowing the application program to be loaded into a memory component for simulation. Thus, Rompaey fails to cure the basic deficiencies of Ball discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is not suggested, disclosed, or taught by Ball and Rompaey, either singly or in combination thereof. As such, the present invention, as defined by independent claims 1, 7, 11, 12, and 15, is patentably distinguishable over Ball and Rompaey. Thus claims 2-6 depending from independent claim 1, claims 8-10 depending from independent claim 7, claims 13-14 depending from independent claim 12, and claims 16-17 depending from independent claim 15 are, *a fortiori*, also patentably distinguishable over Ball and Rompaey for at least

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the reasons presented above and also for additional limitations contained in each dependent claim.

C. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, 11, 12, and 15, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-17 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-17 pending in the present application is respectfully requested.

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